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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/655,910	09/06/2003	David A. Frazer	906-03080601	7676

25864 7590 11/29/2005

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EXAMINER	
CUNNINGHAM, GREGORY F	
ART UNIT	**PAPER NUMBER**
2676	

DATE MAILED: 11/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/655,910	FRAZER ET AL.	
	Examiner	Art Unit	
	Gregory F. Cunningham	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to communications of amendment received 9/15/2005.

2. The disposition of the claims is as follows: claims 1-14 are pending in the application. Claims 1 and 8 are independent claims.

3. When making claim amendments, the applicant is encouraged to consider the references in their entireties, including those portions that have not been cited by the examiner and their equivalents as they may most broadly and appropriately apply to any particular anticipated claim amendments.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harrington (US Patent 5,581,376 A), further in view of Wakasugi (US Patent 6,157,937), further in view of Loewenthal et al. (US Patent 5,712,922 A), hereinafter Loewenthal, and further in view of Inoue (US Patent 6,571,010).

A. Claim 1, "A method for converting an input image with a plurality of pixels to an output image using an N-dimensional conversion table with a plurality of nodes, the method comprising

the steps of [Harrington: abstract; col. 1, lns. 41-62; and col. 3, lns. 39-63; and col. 6, lns. 46-52; and Wakasugi: col. 5, lns. 26-64]:

storing odd-indexed nodes and even-indexed nodes on separate RAMS for each dimension of the conversion table;

retrieving for each pixel a set of output color values corresponding to nodes adjacent to the pixel in the conversion table [Harrington: col. 3, ln. 39 – col. 4, ln. 20; and also Wakasugi: col. 1, lns. 14-39]; and

interpolating within each set of output color values to produce the output image [Harrington: col. 2, lns. 18-47; and also Wakasugi: col. 3, ln. 28 – 67 and col. 5, lns. 26-64]" is disclosed by Harrington [as detailed].

However Harrington and Wakasugi do not appear to disclose "storing odd-indexed nodes and even-indexed nodes on separate RAMS for each dimension of the conversion table", but Wakasugi does teach both the even table and odd table are in memory such as RAM or ROM at col. 8, lns. 34-45 (see Fig. 10 for three-dimensional interpolation); and Loewenthal furthermore demonstrates in col. 11, lns. 6-29 to separate odd and even memory RAM banks as shown in Fig. 5 – see items 90a and 90b.

However Harrington, Wakasugi and Loewenthal do not appear to disclose

"providing an input image to an output image using N-dimensional conversion table with a plurality of nodes, the N-dimensional conversion table being composed of a plurality of at least four subsets each containing color information adapted to be simultaneously obtained

[Inoue – col. 6, lns. 43-59 at 'Thus, in the color conversion table memory 114, it is necessary to provide six memories and to dispose the simultaneously accessed lattice points in

different memories. Therefore, in which of M0 to M5 of the color conversion table memory 114 the data of the 729 lattice points are stored will be described with reference to FIGS. 3(A) to 3(D).

FIG. 3(A) shows the RGB space of the color conversion table memory 114 comprising the 729 lattice points. The spatial axis is (X, Y, Z)=(RH, BH, GH). Consideration is separately given to the three lattice points on the top surface and the three lattice points on the bottom surface of the six lattice points constituting the triangular prism. That is, the planes of GH=0, 2, 4, 6 and 8 (even-numbered planes) are assigned to the color conversion table memories M0 to M2, and the planes of GH=1, 3, 5, and 7 (odd-numbered planes) are assigned to the color conversion table memories M3 to M5.']];

storing odd-indexed nodes and even-indexed nodes respectively on separate RAMS for each dimension of the conversion table[Inoue – supra, col. 6, lns. 43-59];

thereby expediting input conversion using a single access of memory for interpolation of the data points[Inoue – supra, col. 6, lns. 43-59]", but Inoue does [Inoue – as detailed].

Furthermore Inoue's 'six memories as in different memories associated with the planes of GH=0, 2, 4, 6 and 8 (even-numbered planes) are assigned to the color conversion table memories M0 to M2, and the planes of GH=1, 3, 5, and 7 (odd-numbered planes) are assigned to the color conversion table memories M3 to M5' corresponds to any of CRAM, SRAM, ECRAM or RAM.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply 'correcting color images using tetrahedral' disclosed by Harrington and 'high speed interpolation circuit' disclosed by Wakasugi in combination with employing 'even and odd banks in separate RAM' disclosed by Loewenthal, and further coupled with

providing six memories and to dispose the simultaneously accessed lattice points in different memories as disclosed by Inoue, and motivated to combine the teachings because it would 'an interpolation circuit in which miniaturization of circuit scale and high speed processing are attained' as revealed by Wakasugi in col. 1, lns. 9-10, and as revealed by Inoue in col. 2, lns. 60-61 at 'an efficient color conversion table memory is used for a high-speed and high-precision color conversion.

B. Per independent claim 8, this is directed to an apparatus for performing the method of independent claim 1, and therefore is rejected to independent claim 1.

C. Claim 2, "The method according to claim 1 wherein each pixel has N color components" is disclosed, supra for claim 1, by Harrington, Wakasugi, Loewenthal, Inoue and furthermore by Wakasugi in col. 1, lns. 17-19 and col. 5, lns. 26-55.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply 'correcting color images using tetrahedral' disclosed by Harrington and 'N color components' disclosed by Wakasugi in combination with employing 'even and odd banks in separate RAM' disclosed by Loewenthal and Inoue and motivated to combine the teachings because it would 'an interpolation circuit in which miniaturization of circuit scale and high speed processing are attained' as revealed by Wakasugi in col. 1, lns. 9-10.

D. Claim 3, "The method according to claim 2 wherein each color component allocates bits for indexing into the conversion table" is disclosed, supra for claim 2, by Harrington, Wakasugi, Loewenthal, Inoue and furthermore by Wakasugi in col. 7, lns. 27-65

E. Claim 4, "The method according to claim 2 wherein each color component allocates bits for interpolation" is disclosed, supra for claim 2, by Harrington, Wakasugi, Loewenthal, Inoue and furthermore by Wakasugi in col. 7, lns. 27-65.

F. Claim 5, "The method according to claim 1 wherein the set of output values are capable of being simultaneously accessed from the RAMS" is disclosed, supra for claim 1, by Harrington, Wakasugi, Loewenthal, Inoue and furthermore by Wakasugi in col. 8, ln. 57 – col. 9, ln. 13.

G. Claim 6, "The method according to claim 1 wherein the input image is in the RGB color space" is disclosed, supra for claim 1, by Harrington, Wakasugi, Loewenthal, Inoue and furthermore by Harrington in col. 6, ln. 46 – col. 9, ln. 31.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply 'correcting color images using tetrahedral' and 'RGB' disclosed by Harrington and 'high speed interpolation circuit' disclosed by Wakasugi in combination with employing 'even and odd banks in separate RAM' disclosed by Loewenthal and Inoue and motivated to combine the teachings because it would 'an interpolation circuit in which miniaturization of circuit scale and high speed processing are attained' as revealed by Wakasugi in col. 1, lns. 9-10.

H. Claim 7, "The method according to claim 1 wherein the output image is in the CMYK color space" is disclosed, supra for claim 1, by Harrington, Wakasugi, Loewenthal, Inoue and furthermore by Harrington in col. 6, ln. 46 – col. 9, ln. 31.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply 'correcting color images using tetrahedral' and 'CMYK' disclosed

by Harrington and 'high speed interpolation circuit' disclosed by Wakasugi in combination with employing 'even and odd banks in separate RAM' disclosed by Loewenthal, and motivated to combine the teachings because it would 'an interpolation circuit in which miniaturization of circuit scale and high speed processing are attained' as revealed by Wakasugi in col. 1, lns. 9-10.

J. Per dependent claims 9-14, these are directed to an apparatus for performing the method of dependent claims 2-7, and therefore are identically rejected to dependent claims 2-7.

Response to Arguments

6. Substance of the first Office Action, mail date 6/28/2005, used in the rejection is incorporated herein by reference.

17. Applicant's arguments with respect to claims 1-14 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Responses

9. Responses to this action should be mailed to: Commissioner of Patents and Trademarks, Washington, D.C. 20231.

Inquiries

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gregory F. Cunningham whose telephone number is (571) 272-7784.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on (571) 272-7778. The Central FAX Number for the organization where this application or proceeding is assigned is **571-273-8300**.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

G.F. Cunningham

Gregory F. Cunningham
Examiner
Art Unit 2676

gfc

Matthew C. Bella

11/22/2005

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